CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

first, second, and third plane-like metal layers;

a first transistor having a first control terminal, a first terminal that communicates with said second plane-like metal layer and a second terminal that communicates with said first plane-like metal layer;

a second transistor having a second control terminal, a third terminal that communicates with said first plane-like metal layer and a fourth terminal that communicates with said third plane-like metal layer; and

a fourth plane-like metal layer that includes first, second and third contact portions that communicate with said second plane-like metal layer, said first plane-like metal layer and said third plane-like metal layer, respectively.

2. The integrated circuit of Claim 1 wherein said fourth plane-like metal layer is a top layer that is thicker than said first, second and third plane-like metal layers.

3. The integrated circuit of Claim 1 wherein said second and third plane-like metal layers are coplanar.

4. The integrated circuit of Claim 1 wherein said second and third plane-like metal layers are located in separate planes.

5. The integrated circuit of Claim 1 further comprising a plurality of local interconnects that communicate with said first terminal, said second terminal and said first control terminal of said first transistor and said third terminal, said fourth terminal and said second control terminal of said second transistor.

6. The integrated circuit of Claim 1 wherein said first and second transistors are NMOS transistors, said first and second control terminals are gates, said first and third terminals are drains and said second and fourth terminals are sources.

7. The integrated circuit of Claim 1 wherein said first transistor is a PMOS transistor, said second transistor is an NMOS transistor, said first and second control terminals are gates, said first terminal is a source, said second terminal is a drain, said third terminal is a drain, and said fourth terminal is a source.

8. The integrated circuit of Claim 1 wherein said first plane-like metal layer is arranged between said second and third plane-like metal layers and said first and second transistors.

9. The integrated circuit of Claim 1 wherein said second and third plane-like metal layers are arranged between said first plane-like metal layer and said first and second transistors.

10. The integrated circuit of Claim 1 further comprising insulating material that is arranged between said first, second, third and fourth plane-like metal layers.

11. The integrated circuit of Claim 1 wherein said first, second, and third contact portions have an elliptical shape.

12. The integrated circuit of Claim 1 wherein said first, second and third contact portions are generally rectangular and each substantially cover approximately 1/3 of an underlying area defined by said first and second transistors less an area between said first, second and third contact portions.

13. The integrated circuit of Claim 1 wherein one of V_{dd} and V_{ss} is supplied to said first contact portion, the other of said V_{dd} and V_{ss} is supplied to said third contact portion and V_x is output by said second contact portion, wherein a first pair includes said first and second transistors and further comprising second and third pairs of said first and second transistors arranged on opposite sides of said first pair.

14. The integrated circuit of Claim 13 wherein said first contact portion supplies said one of said V_{ss} and V_{dd} to said second transistor of said second pair and said first transistor of said first pair, wherein said third contact portion supplies said other of said V_{ss} and V_{dd} to said second transistor of said first pair and said first transistor of said third pair.

15. The integrated circuit of Claim 1 wherein said first and third contact portions have a base portion and wings that extend from said base portion, and wherein said second contact portions are received between said wings of said first and third contact portions.

16. The integrated circuit of Claim 15 wherein said first, second and third contact portions each substantially cover approximately 1/3 an underlying area defined by said first and second transistors less an area between said first, second and third contact portions.

17. The integrated circuit of Claim 1 wherein a first pair includes said first and second transistors and further comprising second, third and fourth pairs of transistors that are arranged in a generally square arrangement.

18. The integrated circuit of Claim 17 wherein each of said second, third and fourth pairs of transistors include:

a third transistor having a third control terminal, a fifth terminal that communicates with said second plane-like metal layer and a sixth terminal that communicates with said first plane-like metal layer; and

a fourth transistor having a fourth control terminal, a seventh terminal that communicates with said first plane-like metal layer and an eighth terminal that communicates with said third plane-like metal layer.

19. The integrated circuit of Claim 18 wherein said fourth metal layer further includes fourth, fifth, sixth and seventh contact portions, wherein said first, and fourth contact portions have a base portion and wings that extend from said base portion, wherein said third contact portion has a base portion and wings that extend from opposite sides of said base portion, and wherein said second and sixth contact portions are received between said wings of said first and third contact portions, and said fifth and seventh contact portions are received between wings of said third and fourth contact portions.

20. The integrated circuit of Claim 19 wherein said first contact portion supplies one of V_{ss} and V_{dd} to said first and third pairs of transistors, wherein said second contact portion receives V_x from said first pair of transistors, said third contact portion supplies the other of said V_{ss} and V_{dd} to said first, second, third and fourth pairs of transistors, said fourth contact portion supplies said one of said V_{ss} and V_{dd} to said second and fourth pairs of transistors and said fifth, sixth and seventh contact portions receive V_x from said second, third and fourth pairs of transistors, respectively.

21. The integrated circuit of Claim 20 further comprising:

a substrate having first, second, third, fourth, fifth, sixth and seventh transmission lines that are arranged on a first side thereof and that communicate with said first, second, third, fourth, fifth, sixth and seventh contact portions;

eighth, ninth, tenth and eleventh transmission lines arranged on an opposite side of said substrate; and

vias in said substrate connecting said second, fifth, sixth and seventh transmission lines to said eighth, ninth, tenth and eleventh transmission lines.

22. The integrated circuit of Claim 1 wherein said first and third contact portions are generally "C"-shaped and wherein said second contact portion is arranged between said first and third contact portions.

23. The integrated circuit of Claim 1 wherein said second contact portion is generally "H"-shaped and said first and second contact portions are generally rectangular shaped.

24. The integrated circuit of Claim 1 wherein said integrated circuit has a length to width ratio of at least 2:1.

25. The integrated circuit of Claim 1 wherein said integrated circuit implements a power IC, said first contact portion supplies a first voltage potential to said power IC, said third contact portion supplies a second voltage potential to said power IC and said second contact portion receives an output voltage of said power IC.

26. The integrated circuit of Claim 25 wherein said first contact portion supplies V_{ss} to said first and second transistors, said second contract portion receives V_x from said first and second transistors and said third contact portion supplies V_{dd} to said first and second transistors.

27. The integrated circuit of Claim 1 further comprising:

an additional contact portion that is arranged in said fourth plane-like metal layer; and

local interconnects that connect said additional contact portion with at least one of said first and second control terminals of said transistors.

28. A system comprising the integrated circuit of Claim 1 and further comprising a leadframe including first, second and third transmission lines that communicate with said first, second and third contact portions, respectively.

29. The system of Claim 28 wherein said integrated circuit and said first, second and third transmission lines are encased by a mold compound.

30. The system of Claim 28 wherein said leadframe and said integrated circuit implement a quad flat no-lead (QFN) package.

31. A system comprising the integrated circuit of Claim 1 and further comprising:

a first transmission line that communicates with said first contact portion;

a second transmission line that communicates with said second contact portion; and

a third transmission line that communicates with said third contact portion.

32. The system of Claim 31 wherein said first transmission line is connected to V_{ss}, said second transmission line is connected to V_x and said third transmission line is connected to V_{dd}, and wherein said first, second and third transmission lines extend from one side of said integrated circuit.

33. The system of Claim 31 wherein said first transmission line is connected to V_{ss}, said second transmission line is connected to V_x and said third transmission line is connected to V_{dd}, wherein said first and third transmission lines extend from one side of said integrated circuit, and wherein said second transmission line extends from an opposite side of said integrated circuit.

34. The system of Claim 31 further comprising a capacitance that has one end that communicates with said second transmission line and an opposite end that communicates with said third transmission line, wherein said second transmission line supplies a first voltage potential and said third transmission line supplies a second voltage potential.

35. The system of Claim 31 wherein said first transmission line is located in a first layer and wherein said second and third transmission lines are located in a second layer.

36. The system of Claim 31 wherein said first, second and third transmission lines are arranged on a substrate.

37. The integrated circuit of Claim 1 wherein said first, second and third contact portions of said fourth plane-like metal layer substantially overlap an underlying area defined by said first and second transistors.

38. The integrated circuit of Claim 37 wherein said first, second and third contact portions cover approximately 1/3 of said underlying area.

39. The integrated circuit of Claim 1 comprising:

a third transistor having a third control terminal, a fifth terminal that communicates with said second plane-like metal layer and a sixth terminal that communicates with said first plane-like metal layer; and

a fourth transistor having a fourth control terminal, a seventh terminal that communicates with said first plane-like metal layer and an eighth terminal that communicates with said third plane-like metal layer,

wherein said fourth plane-like metal layer includes fourth and fifth contact portions that communicate with said first plane-like metal layer and said second plane-like metal layer, respectively.

40. The integrated circuit of Claim 39 wherein said first contact portion provides one of V_{ss} and V_{dd} to said first and second transistors, said second contact portion receives V_x from said first and second transistors, said third contact portion provides the other of said V_{ss} and V_{dd} to said first, second, third and fourth transistors, said fourth contact portion receives V_x from said third and fourth transistors, and said fifth contact portion provides said one of said V_{ss} and V_{dd} to said third and fourth transistors.

41. The integrated circuit of Claim 39 further comprising:

a first transmission line that communicates with said first contact portion;

a second transmission line that communicates with said second contact portion;

a third transmission line that communicates with said third contact portion;

a fourth transmission line that communicates with said fourth contact portion; and

a fifth transmission line that communicates with said fifth contact portion.

42. The integrated circuit of Claim 41 wherein said first, third and fifth transmission lines are arranged on one side of said integrated circuit and said second and fourth transmission lines are arranged on an opposite side of said integrated circuit.

43. The integrated circuit of Claim 42 wherein a first pitch defined by said first, third and fifth transmission lines is twice a second pitch defined by said first, second, third and fourth transistors.

44. The integrated circuit of Claim 41 further comprising:

additional pairs of transistors arranged adjacent to said first, second, third and fourth transistors for a total of n transistors;

additional contact portions in said fourth metal layer for a total of m contact portions, wherein $m = n + 1$; and

additional transmission lines that are connected to said additional contact portions for a total of m transmission lines.

45. An interconnect structure for connecting a first integrated circuit to a second integrated circuit, comprising:

a first dielectric layer;

a first metal buildup layer arranged on one side of said first dielectric layer;

a second metal layer arranged on an opposite side of said first dielectric layer;

vias connecting said first metal buildup layer to said second metal layer,

wherein said first metal buildup layer defines first, second and third contact portions that are electrically insulated from each other, said first and third contact portions including a base portion and wings that extend from said base portion and said second contact portions are arranged between said wings of said first and third contact portions.

46. The interconnect structure of Claim 45 further comprising:

a solder mask arranged on said second metal layer that defines openings to said second metal layer; and

solder balls that are located in said openings that connect said second metal layer to one of said first and second integrated circuits.

47. The interconnect structure of Claim 45 wherein said vias are laser drilled vias and said first metal buildup layer includes Copper that is electroplated to said first dielectric layer.

48. The interconnect structure of Claim 45 further comprising:

a third metal layer;

a substrate that is arranged between said second metal layer and said third metal layer and that includes plated through holes that connect said second metal layer to said third metal layer;

a second dielectric layer that is arranged adjacent said third metal layer; and

a fourth metal layer that is arranged between said dielectric layer and said solder mask, wherein said second dielectric layer includes laser drilled vias that connect said third metal layer to said fourth metal layer.

49. The interconnect structure of Claim 45 further comprising a capacitor that is connected to said first and third contact portions of said first metal buildup layer.

50. The interconnect structure of Claim 45 further comprising a heat sink that is connected to at least one of said first, second and third contact portions of said first metal buildup layer.

51. The interconnect structure of Claim 45 further comprising a heat sink strap having a first end that is connected to one side of said first integrated circuit and a second end that is connected to said metal buildup layer.

52. The interconnect structure of Claim 45 further comprising:

a stiffening bar that is connected to said metal buildup layer; and

a heat sink strap having a first end that is connected to said metal buildup layer, a midportion that is connected to one side of said first integrated circuit and a second end that is connected to said stiffening bar.

53. The interconnect structure of Claim 45 wherein said first integrated circuit is a power IC and said second integrated circuit is a drive IC.

54. An interconnect structure for connecting a first integrated circuit to a second integrated circuit, comprising:

an aluminum core having first, second and third conducting portions that are defined therein and that are insulated from each other; and

first, second and third inverted vias that are arranged on one side of respective ones of said first, second and third conducting portions.

55. The interconnect structure of Claim 54 further comprising fourth, fifth and sixth inverted vias that are arranged on an opposite side of respective ones of said first, second and third conducting portions.

56. The interconnect structure of Claim 54 further comprising a stiffening material that is arranged between said first, second and third inverted vias.

57. A system comprising said interconnect structure of Claim 54 and said first and second integrated circuits, wherein said first integrated circuit includes first, second and third contact portions that communicate with said first, second and third inverted vias and wherein said second integrated circuit includes fourth, fifth and sixth contact portions that communicate with said fourth, fifth and sixth inverted vias.

58. A circuit, comprising:

a first integrated circuit that comprises a top plane-like metal layer with first, second and third contact portions, wherein said first and third contact portions include a first base and first wings that extend from said first base, and wherein said second contact portions are arranged between said first wings of said first and third contact portions; and

an interconnect structure that communicates with said first integrated circuit and that includes a first metal buildup layer with fourth, fifth and sixth contact portions, wherein said fourth and sixth contact portions include a second base and second wings that extend from said second base, and wherein said fifth contact portions are arranged between said wings of said fourth and sixth contact portions.

59. The circuit of Claim 58 wherein said second bases of said fourth and sixth contact portions extend beyond said first bases of said first and third contact portions.

60. The circuit of Claim 58 wherein said second and fifth contact portions, said first wings of said first and third contact portions, and said second wings of said fourth and sixth contact portions substantially align with each other.

61. The circuit of Claim 58 wherein said first bases of said first and third contact portions align with said second bases of said fourth and sixth contact portions.

62. The circuit of Claim 58 wherein a side of said second bases of said fourth and sixth contact portions extends beyond said first bases of said first and third contact portions, respectively.

63. The circuit of Claim 58 wherein said integrated circuit includes:

a first transistor having a first control terminal, a first terminal that communicates with said second plane-like metal layer and a second terminal that communicates with said first plane-like metal layer;

a second transistor having a second control terminal, a third terminal that communicates with said first plane-like metal layer and a fourth terminal that communicates with said third plane-like metal layer; and

a fourth plane-like metal layer that includes first, second and third contact portions that are electrically isolated from each other and that communicate with said second plane-like metal layer, said first plane-like metal layer and said third plane-like metal layer, respectively.

64. The circuit of Claim 63 wherein said fourth plane-like metal layer is a top layer that is thicker than said first, second and third plane-like metal layers.

65. The circuit of Claim 63 wherein said second and third plane-like metal layers are coplanar.

66. The circuit of Claim 63 wherein said second and third plane-like metal layers are located in separate planes.

67. The circuit of Claim 63 further comprising local interconnects that communicate with said first terminal, said second terminal and said first control terminal of said first transistor and said third terminal, said fourth terminal and said second control terminal of said second transistor.

68. The circuit of Claim 63 wherein said first and second transistors are NMOS transistors, said first and second control terminals are gates, said first and third terminals are drains and said second and fourth terminals are sources.

69. The circuit of Claim 63 wherein said first transistor is a PMOS transistor, said second transistor is an NMOS transistor, said first and second control terminals are gates, said first terminal is a source, said second terminal is a drain, said third terminal is a drain, and said fourth terminal is a source.

70. The circuit of Claim 63 wherein said first plane-like metal layer is arranged between said second and third plane-like metal layers and said first and second transistors.

71. The circuit of Claim 63 wherein said second and third plane-like metal layers are arranged between said first plane-like metal layer and said first and second transistors.

72. The circuit of Claim 63 further comprising insulating material that is arranged between said first, second, third and fourth plane-like metal layers.

73. The circuit of Claim 58 wherein said first, second, and third contact portions have an elliptical shape.

74. The circuit of Claim 63 wherein said first, second and third contact portions are generally rectangular and each substantially cover approximately 1/3 of an underlying area defined by said first and second transistors less an area between said first, second and third contact portions.

75. The circuit of Claim 63 wherein one of V_{dd} and V_{ss} is supplied to said first contact portion, the other of said V_{dd} and V_{ss} is supplied to said third contact portion and V_x is output by said second contact portion, wherein a first pair includes said first and second transistors and further comprising second and third pairs of said first and second transistors arranged on opposite sides of said first pair.

76. The circuit of Claim 75 wherein said first contact portion supplies said one of said V_{ss} and V_{dd} to said second transistor of said second pair and said first transistor of said first pair, wherein said third contact portion supplies said other of said V_{ss} and V_{dd} to said second transistor of said first pair and said first transistor of said third pair.

77. The circuit of Claim 58 wherein said first and third contact portions have a base and wings that extend from said base, wherein said second contact portions are received between said wings of said first and third contact portions.

78. The circuit of Claim 77 wherein said first, second and third contact portions each substantially cover approximately 1/3 an underlying area defined by said first and second transistors less an area between said first, second and third contact portions.

79. The circuit of Claim 63 wherein a first pair includes said first and second transistors and further comprising second, third and fourth pairs of transistors that are arranged in a generally square arrangement.

80. The circuit of Claim 79 wherein each of said second, third and fourth pairs of transistors include:

a third transistor having a third control terminal, a fifth terminal that communicates with said second plane-like metal layer and a sixth terminal that communicates with said first plane-like metal layer; and

a fourth transistor having a fourth control terminal, a seventh terminal that communicates with said first plane-like metal layer and an eighth terminal that communicates with said third plane-like metal layer.

81. The circuit of Claim 80 wherein said fourth metal layer further includes fourth, fifth, sixth and seventh contact portions, wherein said first, and fourth contact portions have a base portion and wings that extend from said base portion, wherein said third contact portion has a base portion and wings that extend from opposite sides of said base portion, and wherein said second and sixth contact portions are received between said wings of said first and third contact portions, and said fifth and seventh contact portions are received between wings of said third and fourth contact portions.

82. The circuit of Claim 81 wherein said first contact portion supplies one of V_{ss} and V_{dd} to said first and third pairs of transistors, wherein said second contact portion receives V_x from said first pair of transistors, said third contact portion supplies the other of V_{ss} and V_{dd} to said first, second, third and fourth pairs of transistors, said fourth contact portions supplies said one of said V_{ss} and V_{dd} to said second and fourth pairs of transistors and said fifth, sixth and seventh contact portions receive V_x from said second, third and fourth pairs of transistors.

83. The circuit of Claim 82 further comprising:

a substrate having first, second, third, fourth, fifth, sixth and seventh transmission lines that are arranged on a first side thereof and that communicate with said first, second, third, fourth, fifth, sixth and seventh contact portions;

eighth, ninth, tenth and eleventh transmission lines arranged on an opposite side of said substrate; and

vias in said substrate connecting said second, fifth, sixth and seventh transmission lines to said eighth, ninth, tenth and eleventh transmission lines.

84. The circuit of Claim 58 wherein said first and third contact portions are generally "C"-shaped and wherein said second contact portion is arranged between said first and third contact portions.

85. The circuit of Claim 58 wherein said second contact portion is generally "H"-shaped and said first and third contact portions are generally rectangular shaped.

86. The circuit of Claim 58 wherein said integrated circuit has a length to width ratio of at least 2:1.

87. The circuit of Claim 58 wherein said integrated circuit implements a power IC, said first contact portion supplies a first voltage potential to said power IC, said third contact portion supplies a second voltage potential to said power IC and said second contact portion receives an output voltage of said power IC.

88. The circuit of Claim 63 wherein said first contact portion supplies V_{ss} to said first and second transistors, said second contract portion receives V_x from said first and second transistors and said third contact portion supplies V_{dd} to said first and second transistors.

89. The circuit of Claim 63 further comprising:

an additional contact portion arranged in said fourth plane-like metal layer; and

local interconnects that connect said additional contact portion to at least one of said first and second control terminals of said first and second transistors.

90. The circuit of Claim 58 wherein said interconnect structure includes:

a first dielectric layer having said first metal buildup layer arranged on one side thereof;

a second metal layer arranged on an opposite side of said first dielectric layer; and

a plurality of vias connecting said first metal buildup layer to said second metal buildup layer.

91. The circuit of Claim 90 further comprising:

a solder mask arranged on said second metal layer that defines openings to said second metal layer; and

solder balls that are located in said openings that connect said second metal layer to one of said first and second integrated circuits.

92. The circuit of Claim 90 wherein said vias are laser drilled vias and said first metal buildup layer includes Copper that is electroplated to said first dielectric layer.

93. The circuit of Claim 90 further comprising:

a third metal layer;

a substrate that is arranged between said second metal layer and said third metal layer and that includes plated through holes that connect said second metal layer to said third metal layer;

a second dielectric layer that is arranged adjacent said third metal layer; and

a fourth metal layer that is arranged between said dielectric layer and said solder mask, wherein said second dielectric layer includes laser drilled vias that connect said third metal layer to said fourth metal layer.

94. The circuit of Claim 58 further comprising a capacitor that communicates with said first and third contact portions of said first metal buildup layer.

95. The circuit of Claim 58 further comprising a heat sink that communicates with said first metal buildup layer.

96. A method for reducing parasitic resistance in an integrated circuit, comprising:

connecting first and second terminals of a first transistor to second and first plane-like metal layers, respectively;

connecting third and fourth terminals of a second transistor to said first and a third plane-like metal layer, respectively; and

connecting first, second and third contact portions of a fourth plane-like metal layer to said second plane-like metal layer, said first plane-like metal layer and said third plane-like metal layer, respectively.

97. The method of Claim 96 wherein said fourth plane-like metal layer is thicker than said first, second and third plane-like metal layers.

98. The method of Claim 96 wherein said second and third plane-like metal layers are coplanar.

99. The method of Claim 96 further comprising arranging said second and third plane-like metal layers in separate planes.

100. The method of Claim 96 further comprising using local interconnects to provide connections to said first terminal, said second terminal, and said first control terminal of said first transistor and said third terminal, said fourth terminal, and said second control terminal, respectively, of said second transistor.

101. The method of Claim 96 wherein said first and second transistors are NMOS transistors, said first and second control terminals are gates, said first and third terminals are drains and said second and fourth terminals are sources.

102. The method of Claim 96 wherein said first transistor is a PMOS transistor, said second transistor is an NMOS transistor, said first and second control terminals are gates, said first terminal is a source, said second terminal is a drain, said third terminal is a drain, and said fourth terminal is a source.

103. The method of Claim 96 further comprising arranging said first plane-like metal layer between said second and third plane-like metal layers and said first and second transistors.

104. The method of Claim 96 further comprising arranging said second and third plane-like metal layers between said first plane-like metal layer and said first and second transistors.

105. The method of Claim 96 further comprising insulating said first, second, third and fourth plane-like metal layers.

106. The method of Claim 96 wherein said first, second, and third contact portions have an elliptical shape.

107. The method of Claim 96 wherein said first and third contact portions have a base and wings that extend from said base and further comprising arranging said second contact portions between said wings of said first and third contact portions.

108. The method of Claim 96 wherein said first and third contact portions are generally "C"-shaped and further comprising arranging said second contact portion between said first and third contact portions.

109. The method of Claim 96 wherein said second contact portion is generally "H"-shaped and said first and second contact portions are generally rectangular shaped.

110. The method of Claim 96 wherein said integrated circuit has a length to width ratio of at least 2:1.

111. The method of Claim 96 wherein said integrated circuit implements a power IC and further comprising:

supplying a first voltage potential to said power IC using said first contact portion;

supplying a second voltage potential to said power IC using said third contact portion; and

outputting an output voltage of said power IC at said second contact portion.

112. The method of Claim 96 further comprising:

providing an additional contact portion in said fourth plane-like metal layer; and

using vias and local interconnects to connect said additional contact portion with at least one of said first and second control terminals of said transistors.

113. The method of Claim 96 further comprising connecting first, second and third transmission lines of a leadframe to said first, second and third contact portions, respectively.

114. The method of Claim 113 further comprising encasing said integrated circuit and said first, second and third transmission lines in a mold compound.

115. The method of Claim 113 wherein said leadframe and said integrated circuit implement a quad flat no-lead (QFN) package.

116. The method of Claim 96 further comprising providing an external connection to said integrated circuit using first, second and third transmission lines that communicate with said first, second and third contact portions, respectively.

117. The method of Claim 116 further comprising connecting one end of a capacitance to said second transmission line and an opposite end to said third transmission line, wherein said second transmission line supplies a first voltage potential and said third transmission line supplies a second voltage potential.

118. The method of Claim 116 further comprising locating said first transmission line in a first layer and said second and third transmission lines in a second layer.

119. The method of Claim 116 further comprising arranging said first, second and third transmission lines on a substrate.

120. The method of Claim 96 wherein said first, second and third contact portions of said fourth plane-like metal layer substantially overlap an underlying area defined by said first and second transistors.

121. The method of Claim 120 wherein said first, second and third contact portions substantially cover approximately 1/3 of said underlying area less space between said first, second, and third contact portions.

122. The method of Claim 96 wherein said first, second and third contact portions are generally rectangular and further comprising substantially covering approximately 1/3 of an underlying area defined by said first and second transistors using said first, second and third contact portions less an area between said first, second and third contact portions.

123. The method of Claim 96 further comprising:

supplying one of V_{dd} and V_{ss} to said first contact portion;

supplying the other of said V_{dd} and V_{ss} to said third contact portion;

outputting V_x at said second contact portion, wherein a first pair includes said first and second transistors; and

arranging second and third pairs of said first and second transistors on opposite sides of said first pair.

124. The method of Claim 123 further comprising:

supplying said one of said V_{ss} and V_{dd} to said second transistor of said second pair and said first transistor of said first pair using said first contact portion; and

supplying said other of said V_{ss} and V_{dd} to said second transistor of said first pair and said first transistor of said third pair using said third contact portion.

125. The method of Claim 96 wherein a first pair includes said first and second transistors and further comprising arranging second, third and fourth pairs of transistors in a generally square arrangement.

126. The method of Claim 125 further comprising:

connecting fifth and sixth terminals of a third transistor to said second and first plane-like metal layers, respectively; and

connecting seventh and eighth terminals of a fourth transistor to said first and third plane-like metal layers, respectively.

127. The method of Claim 126 further comprising providing fourth, fifth, sixth and seventh contact portions in said fourth plane-like metal layer, wherein said first, and fourth contact portions have a base portion and wings that extend from said base portion, wherein said second contact portion has a base portion and wings that extend from opposite sides of said base portion, and wherein said second and sixth contact portions are received between said wings of said first and third contact portions, and said fifth and seventh contact portions are received between wings of said third and fourth contact portions.

128. The method of Claim 127 further comprising:

supplying one of V_{ss} and V_{dd} to said first and third pairs of transistors using said first contact portion;

outputting V_x from said first pair of transistors at said second contact portion;

supplying the other of V_{ss} and V_{dd} to said first, second, third and fourth pairs of transistors using said third contact portion;

supplying said one of said V_{ss} and V_{dd} to said second and fourth pairs of transistors using said fourth contact portion; and

outputting V_x from said second, third and fourth pairs of transistors using said fifth, sixth and seventh contact portions, respectively.

129. The method of Claim 128 further comprising:

arranging first, second, third, fourth, fifth, sixth and seventh transmission lines on a first side of a substrate; and

connecting said first, second, third, fourth, fifth, sixth and seventh transmission lines to said first, second, third, fourth, fifth, sixth and seventh contact portions;

arranging eighth, ninth, tenth and eleventh transmission lines on an opposite side of said substrate; and

connecting said second, fifth, sixth and seventh transmission lines through said substrate to said eighth, ninth, tenth and eleventh transmission lines.

130. The method of Claim 96 further comprising:

supplying one of V_{ss} and V_{dd} to a first transmission line that is connected to said first contact portion;

outputting V_x using a second transmission line to that is connected to said second contact portion; and

supplying the other of said V_{ss} and V_{dd} to a third transmission line that is connected to said third contact portion, wherein said first, second and third transmission lines extend from one side of said integrated circuit.

131. The method of Claim 96 further comprising:

supplying one of V_{ss} and V_{dd} to a first transmission line that is connected to said first contact portion;

outputting V_x using a second transmission line to that is connected to said second contact portion; and

supplying the other of said V_{ss} and V_{dd} to a third transmission line that is connected to said third contact portion, wherein said first and third transmission lines extend from one side of said integrated circuit, and wherein said second transmission line extends from an opposite side of said integrated circuit.

132. The method of Claim 96 comprising:

connecting fifth and sixth terminals of a third transistor to said second plane-like metal layer and said first plane-like metal layer, respectively;

connecting seventh and eighth terminals of a fourth transistor to said first plane-like metal layer and said third plane-like metal layer, respectively; and

connecting fourth and fifth contact portions to said first plane-like metal layer and said second plane-like metal layer, respectively.

133. The method of Claim 132 further comprising:

supplying V_{ss} to said first and second transistors using said first contact portion;

outputting V_x from said first and second transistors using said second contact portion;

supplying V_{dd} to said first, second, third and fourth transistors using said third contact portion;

outputting V_x from said third and fourth transistors using said fourth contact portion; and

supplying V_{ss} to said third and fourth transistors using said fifth contact portion.

134. The method of Claim 132 further comprising:

connecting a first transmission line to said first contact portion;

connecting a second transmission line to said second contact portion;

connecting a third transmission line to said third contact portion;

connecting a fourth transmission line to said fourth contact portion; and

connecting a fifth transmission line to said fifth contact portion.

135. The method of Claim 134 further comprising:

arranging said first, third and fifth transmission lines on one side of said integrated circuit; and

arranging said second and fourth transmission lines on an opposite side of said integrated circuit.

136. The method of Claim 135 wherein a first pitch defined by said first, third and fifth transmission lines and said second and fourth transmission lines is twice a second pitch defined by said first, second, third and fourth transistors.

137. A method for providing an interconnect structure for connecting a first integrated circuit to a second integrated circuit, comprising:

providing a first dielectric layer;

forming a first metal buildup layer on one side of said first dielectric layer;

forming a second metal layer on an opposite side of said first dielectric layer;

using vias to connect said first metal buildup layer to said second metal layer,

defining first, second and third contact portions in said first metal buildup layer that are electrically insulated from each other, wherein said first and third contact portions include a base and wings that extend from said base and said second contact portions are arranged between said wings of said first and third contact portions.

138. The method of Claim 137 further comprising:

providing a solder mask on said second metal layer to define openings to said second metal layer; and

locating solder balls in said openings that connect said second metal layer to one of said first and second integrated circuits.

139. The method of Claim 137 further comprising:

laser drilling said vias; and

electroplating Copper to said first dielectric layer to form said first metal buildup layer.

140. The method of Claim 137 further comprising connecting a capacitor to said first and third contact portions of said first metal buildup layer.

141. The method of Claim 137 further comprising connecting a heat sink to said first metal buildup layer.

142. The method of Claim 137 wherein said first integrated circuit is a power IC and said second integrated circuit is a drive IC.

143. A method for providing an interconnect structure for connecting a first integrated circuit to a second integrated circuit, comprising:

defining first, second and third conducting portions in an aluminum core, wherein said first, second and third conducting portions are insulated from each other; and

forming first, second and third inverted vias on one side of respective ones of said first, second and third conducting portions.

144. The method of Claim 143 further comprising forming fourth, fifth and sixth inverted vias on an opposite side of respective ones of said first, second and third conducting portions.

145. The method of Claim 143 further comprising applying a stiffening material between said first, second and third inverted vias.

146. The method of Claim 143 wherein said first integrated circuit includes first, second and third contact portions and said second integrated circuit includes fourth, fifth and sixth contact portions and further comprising:

connecting said first, second and third inverted vias to said first, second and third contact portions; and

connecting said fourth, fifth and sixth inverted vias to said fourth, fifth and sixth contact portions.

147. The integrated circuit of Claim 1 wherein each of said first, second and third plane-like metal layers cover greater than approximately 80% of both of said underlying first and second transistors.

148. The integrated circuit of Claim 1 wherein said first plane-like metal layer covers greater than approximately 80% of both of said underlying first and second transistors and wherein said second and third plane-like metal layers cover greater than approximately 80% of said first and second transistors, respectively.

149. The circuit of Claim 63 wherein said first, second and third plane-like metal layers each cover greater than approximately 80% of both of said underlying first and second transistors.

150. The circuit of Claim 63 wherein said first plane-like metal layer covers greater than approximately 80% of both of said underlying first and second transistors and wherein said second and third plane-like metal layers cover greater than approximately 80% of said first and second transistors, respectively.

151. The method of Claim 96 wherein said first, second and third plane-like metal layers each cover greater than approximately 80% of both of said underlying first and second transistors.

152. The method of Claim 96 wherein said first plane-like metal layer covers greater than approximately 80% of both of said underlying first and second transistors and wherein said second and third plane-like metal layers cover greater than approximately 80% of said first and second transistors, respectively.

153. The integrated circuit of Claim 1 wherein said first, second and third plane-like metal layers allow current to flow in both x and y directions, wherein said x direction is orthogonal to said y direction.

154. The circuit of Claim 63 wherein said first, second and third plane-like metal layers allow current to flow in both x and y directions, wherein said x direction is orthogonal to said y direction.

155. The method of Claim 96 wherein said first, second and third plane-like metal layers allow current to flow in both x and y directions, wherein said x direction is orthogonal to said y direction.